Amendments to the Claims:

This listing of the claims replaces all prior versions, and listings, of the claims in the application.

Listing of Claims:

1. (Currently amended) An automated method for designing integrated circuits ~~(ICs)~~, comprising the steps of:

describing ~~the l~~an integrated circuit (IC), the description including at least one design objective of said IC;

partitioning said description into at least one functional block, said functional block comprising at least one predefined cell; and

generating at least one design-specific cell representative of said at least one predefined cell of said functional block, wherein said design-specific cell is ~~transistor-level cell and said design-specific cell is~~ generated, characterized and/or optimized at the transistor level based on said design objective of said IC.

2. (Previously presented) The method of claim 1, wherein said step of generating comprises evaluating said design-specific cell based on a context of use for said design-specific cell.

3. (Previously presented) The method of claim 1, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

4. (Previously presented) The method of claim 3, wherein said step of characterizing and selecting is repeated until the design objective is met.

5. (Previously presented) The method of claim 1, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

6. (Original) The method of claim 1, further comprising a step of optimizing said IC design.

7. (Currently Amended) The method of claim 6, wherein a design metric~~criteria~~ for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

8. (Original) The method of claim 6, wherein said step of optimizing is performed automatically.

9. (Currently Amended) The method of claim ~~8~~7, wherein said optimizing is repeated until said IC design meets at least one design metric.

10. (Canceled)

11. (Currently amended) A system for implementing an automated integrated circuit ~~(IC)~~ design process, said system comprising:

a description of ~~said~~an integrated circuit (IC) ~~IC~~, said description including at least one design objective of said IC;

a local optimization control for partitioning said description into at least one functional block, said functional block comprising at least one predefined cell; and

a design-specific cell generator for generating at least one design-specific cell representation of said at least one predefined cell of saidthe functional block, wherein said design-specific cell is ~~a transistor-level cell and said design-specific cell is~~ generated, characterized and/or optimized at the transistor level based on said design objective of said IC.

12. (Previously presented) The system of claim 11, further comprising an analysis control module for evaluating said design-specific cell based on a context of use for said design-specific cell .

13. (Previously presented) The system of claim 11, further comprising a control module for characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

14. (Currently Amended) The system of claim 13, wherein said ~~control module for~~ characterizing and selecting is repeated until said design objective is satisfied.

15. (Previously presented) The system of claim 11, wherein said design-specific cell generator selects said design objective from a group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability, and cost.

16. (Previously presented) The system of claim 11, further comprising an optimizer for optimizing said IC design.

17. (Currently Amended) The system of claim 16, wherein a design metric criteria used by said optimizer is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

18. (Previously presented) The system of claim 16, wherein said optimizer is operated automatically.

19. (Currently Amended) The system of claim 176, wherein said optimizer is iteratively operated until said IC design meets at least one design metric.

20. (Canceled)

21. (Currently amended) A design-specific cell produced by an automated ~~ic~~integrated circuit design process, said ~~ic~~integrated circuit design process comprising:

describing an integrated circuit (IC)~~the IC~~, the description including at least one design objective of said IC;

partitioning said description into at least one functional block, said functional block comprising at least one predefined cell; and

generating at least one design-specific cell representative of said at least one predefined cell of said functional block, wherein said design-specific cell generator generates, characterizes and/or optimizes a transistor-level design-specific cell ~~and said design-specific cell is generated~~ based on the design objective of said IC.

22. (Currently Amended) The design-specific cell produced by said IC design process of claim 21, wherein said IC design process further comprises evaluating said design-specific cell based on a context of use for said design-specific cell-.

23. (Previously presented) The design-specific cell produced by said IC design process of claim 21, wherein said IC design process characterizes and selects said design-specific cell from a minimal set comprising at least one design-specific cell, based on said IC design objective.

24. (Previously presented) The design-specific cell produced by said IC design process of claim 23, wherein said IC design process is repeated until said design objective is met.

25. (Previously presented) The design-specific cell produced by said IC design process of claim 21, wherein said design objective of said IC design process is selected from the group consisting of: IC design die size, die area, performance, power consumption, signal integrity, routability, fault tolerance, testability, reliability, and cost.

26. (Original) The design-specific cell produced by said IC design process of claim 21, wherein said IC design process further comprises a step of optimizing said IC design.

27. (Currently Amended) The design-specific cell produced by said IC design process of claim 26, wherein a design metric~~criteria~~ for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

28. (Original) The design-specific cell produced by said IC design process of claim 21, wherein said step of optimizing is performed automatically.

29. (Currently Amended) The design-specific cell produced by said IC design process of claim 2 ~~7~~8, wherein said step of optimizing is repeated until said IC design satisfies at least one design metric.

30. (Currently amended) A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit ~~(IC)~~, said storage medium comprising:

program instructions for describing ~~the~~ ~~l~~can integrated circuit (IC), the description including at least one design objective of said IC;

program instructions for partitioning said description into at least one functional block, said functional block comprising at least one predefined cell; and

program instructions for generating at least one design-specific cell representative of said at least one predefined cell of ~~the~~said functional block, wherein said design-specific cell generator generates, characterizes and/or optimizes a transistor-level design-specific cell ~~and said design-specific cell is generated~~ based on the design objective of said IC.

31. (Currently amended) An automated method for designing integrated circuits ~~(ICs)~~, comprising the steps of:

describing ~~the~~ ~~l~~can integrated circuit (IC), the description including at least one design objective of said IC;

partitioning said description into at least one functional block, said functional block comprising at least one predefined cell;

generating at least one design-specific cell representative of said at least one predefined cell of said functional block, said design-specific cell is generated, characterized and/or optimized at the transistor level based on said design objective of said IC; and

automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one design metric.

32. (Previously amended) The method of claim 31, wherein said step of generating comprises evaluating said design-specific cell based on a context of use for said design-specific cell.

33. (Previously amended) The method of claim 31, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

34. (Previously amended) The method of claim 33, wherein said step of characterizing and selecting is repeated until the design objective is met.

35. (Previously amended) The method of claim 31, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

36. (Currently Amended) The method of claim 31, wherein a said design metric ~~criteria~~ for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault

tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

37. (Canceled)

38. (Previously amended) The method of claim 31, wherein said design-specific cell is a transistor-level cell.

39. (Currently amended) A system for implementing an automated integrated circuit ~~(IC)~~ design process, said system comprising:

a description of ~~said Ic~~an integrated circuit (IC), said description including at least one design objective of said IC;

a local optimization control for partitioning said description into at least one functional block, said functional block comprising at least one predefined cell;

a design-specific cell generator for generating at least one design-specific cell representation of said at least one predefined cell of said ~~the~~ functional block, said design-specific cell is generated, characterized and/or optimized at the transistor level based on said design objective of said IC; and

an optimizer for automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one design metric.

40. (Previously amended) The system of claim 39, further comprising an analysis control module for evaluating said design-specific cell based on a context of use for said design-specific cell.

41. (Previously amended) The system of claim 39, further comprising a control module for characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

42. (Currently Amended) The system of claim 41, wherein said ~~control module~~characterizing and selecting is repeated until said design objective is satisfied.

43. (Previously amended) The system of claim 39, wherein said design-specific cell generator selects said design objective from a group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability, and cost.

44. (Previously amended) The system of claim 39, wherein a criteria used by said optimizer is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

45. (Canceled)

46. (Previously amended) The system of claim 39, wherein said design-specific cell generator generates a transistor-level design-specific cell.

47. (Currently amended) A design-specific cell produced by an automated ~~ic~~integrated circuit design process, said ~~ic~~integrated circuit design process comprising:

describing ~~the ic~~an integrated circuit (IC), the description including at least one design objective of said IC;

partitioning said description into at least one functional block, said functional block comprising at least one predefined cell;

generating at least one design-specific cell representative of said at least one predefined cell of said functional block, said design-specific cell is generated, characterized and/or optimized at the transistor level based on the design objective of said IC; and

automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one design metric.

48. (Previously amended) The design-specific cell produced by said IC design process of claim 47, wherein said IC design process further comprises evaluating said design-specific cell based on a context of use for said design-specific cell .

49. (Previously amended) The design-specific cell produced by said IC design process of claim 47, wherein said IC design process characterizes and selects said design-specific cell from a minimal set comprising at least one design-specific cell, based on said IC design objective.

50. (Previously amended) The design-specific cell produced by said IC design process of claim 49, wherein said IC design process is repeated until said design objective is met.

51. (Previously amended) The design-specific cell produced by said IC design process of claim 47, wherein said design objective of said IC design process is selected from the group consisting of: IC design die size, die area, performance, power consumption, signal integrity, routability, fault tolerance, testability, reliability, and cost.

52. (Currently Amended) The design-specific cell produced by said IC design process of claim 47, wherein said ~~a criteria~~design metric for said optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

53. (Canceled)

54. (Currently amended) A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit ~~(IC)~~, said storage medium comprising:

program instructions for describing ~~the I~~can integrated circuit (IC), the description including at least one design objective of said IC;

program instructions for partitioning said description into at least one functional block, said functional block comprising at least one predefined cell; and

program instructions for generating at least one design-specific cell representative of said at least one predefined cell of said~~the~~ functional block, said design-specific cell is generated, characterized and/or optimized at the transistor level based on the design objective of said IC; and

program instructions for automatically optimizing said IC design, wherein said optimizing is repeated until said IC design meets at least one design metric.

55. (Previously amended) The storage medium of claim 54, wherein said program instructions for generating comprises program instructions for evaluating said design-specific cell based on a context of use for said design-specific cell.

56. (Previously amended) The storage medium of claim 54, wherein said program instructions for generating comprises program instructions for characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

57. (Previously amended) The storage medium of claim 56, wherein said program instructions for characterizing and selecting is repeated until the design objective is met.

58. (Previously amended) The storage medium of claim 54, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

59. (Previously amended) The storage medium of claim 54, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

60. (Canceled)

61. (Previously amended) The storage medium of claim 54, wherein said design-specific cell is a transistor-level cell.

62. (Previously Presented) The storage medium of claim 30, wherein said program instructions for generating comprises program instructions for evaluating said design-specific cell based on a context of use for said design-specific cell.

63. (Previously Presented) The storage medium of claim 30, wherein said program instructions for generating comprises program instructions for characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective.

64. (Previously Presented) The storage medium of claim 63, wherein said program instructions for characterizing and selecting is repeated until the design objective is met.

65. (Previously Presented) The storage medium of claim 30, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

66. (Previously Presented) The storage medium of claim 30, further comprising a step of optimizing said IC design.

67. (Currently Amended) The storage medium of claim 66, wherein a ~~criteria~~ design metric for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

68. (Currently Amended) The storage medium of claim 67~~6~~, wherein said step of optimizing is performed automatically.

69. (Previously Presented) The storage medium of claim 68, wherein said optimizing is repeated until said IC design meets at least one design metric.

70. (New) The method of claim 1, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

71. (New) The system of claim 11, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

72. (New) The design-specific cell of claim 21, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

73. (New) The storage medium of claim 30, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

74. (New) The method of claim 31, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

75. (New) The system of claim 39, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

76. (New) The design-specific cell of claim 47, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.

77. (New) The storage medium of claim 54, wherein said design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.